# Electronics

# ACORN GOES TO MARKET WITH RISC MICROPROCESSOR

***The British company ships samples of what could be the first commercial RISC chip***

**CAMBRIDGE, ENGLAND**

It has taken a four-man team at Acorn Computers Ltd. just 18 months to develop a 32-bit single-chip microprocessor that executes 3 million instructions/s. Using a reduced-instruction-set-computer architecture to gain performance, Acorn's ARM chip (for Acorn RISC machine) is arguably the industry's first commercial RISC microprocessor.

Acorn is offering the ARM chip on an evaluation board that runs as a second processor linked to its Model B personal computer. Limited samples of this board are available for about $2,000.

Inmos International plc, London, whose transputer chip is also based on a RISC architecture, expects to ship evaluation boards later this year.

Pioneered at Stanford University, the University of California at Berkeley, and IBM Corp.'s Thomas J. Watson Research Center, RISC machines—like race cars—are stripped to the bare essentials and their critical subsystems tuned for high performance. The ARM chip's equivalents of a race car's engine and carburetion system are a pipelined central processing unit and a memory-to-processor port with an exceptionally high bandwidth.

The ARM processor comprises an arithmetic-logic unit, a barrel shifter to assist register operations, and a bank of 25 registers, each 32 bits wide. Acorn tunes the very large-scale integrated circuit for performance in several ways.

First, Acorn hardwires the instruction set, which consists of five basic instruction types, each with an associated condition code. Microprogramming, used in most conventional processors, works by interpreting high-level instructions as a series of microinstructions held in read-only memory. Because this takes several lookup operations, microprogrammed instructions take several cycles. The ARM processor, however, executes any instruction in a single 150-ns clock cycle.

By pipelining, all parts of the processor and memory system can be used every cycle when executing consecutive register-to-register instructions. This means that in any clock cycle, one instruction could control the data path while a second is being decoded for the following cycle and a third is being fetched from memory.

The ARM has a 26-bit address bus and a 32-bit data bus so that it can achieve an 18-megabyte/s memory bandwidth. In comparison, the Digital Equipment Corp. VAX-11/750 and the National Semiconductor Corp. 32016 both offer 4-megabyte/s bandwidths. The ARM has an optional page mode that can increase data-transfer rates another 30%.

Besides being faster than microprocessors of conventional architecture, RISC chips are smaller and thus cheaper to design and make. "We get better performance than a Motorola or Zilog with about one tenth the number of components and a much smaller chip," says Steve Furber, senior designer at Acorn's Business Division.

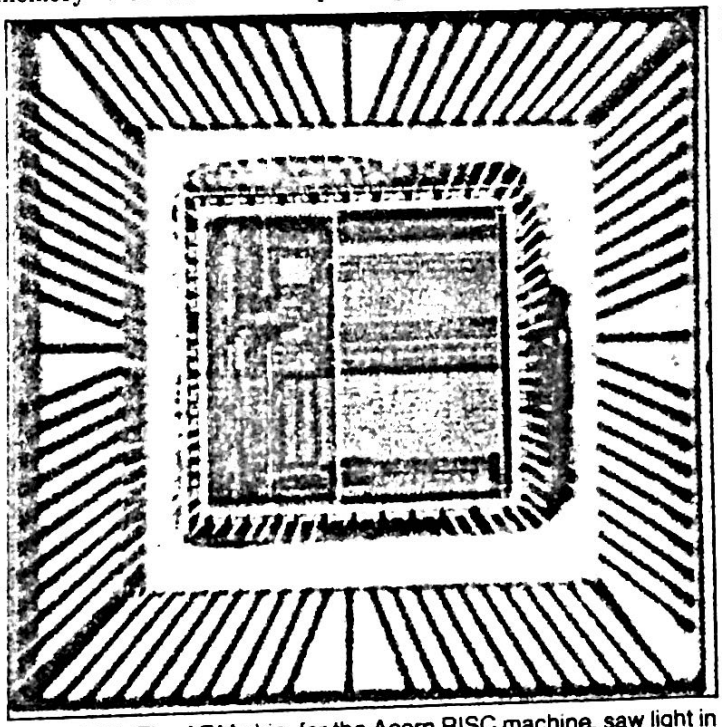
The division's VLSI design team created the ARM chip using software tools provided by VLSI Technology Inc., San Jose, Calif., and fabricated it in that company's low-power 3-$\mu$m double-layer-metal CMOS process. The setup delivered first-time-right silicon in April.

The ARM chip packs 25,000 transistors onto a small 50-mm$^2$ chip. In contrast, Motorola packed about 192,000 devices onto an 80-mm$^2$ chip using 2-$\mu$m design rules to build the 2.5-mips 68020 microprocessor. Acorn's smaller chip improves yields and lowers chip costs by about a factor of four. The company plans a further reduction to 2-$\mu$m design rules, which could increase the cost advantage over conventional processors by a full order of magnitude. Acorn expects to sell the chip in volume for about one third the price of equivalent 32-bit products.

**OUTSTANDING PERFORMANCE.** The ARM processor on the evaluation board transforms the $300 to $400 Model B computer into a professional work station of eye-opening performance. The 6502-based Model B connects to the ARM processor through a high-speed data channel called a tube [*Electronics*, April 5, 1984, p. 74]. The Model B takes care of all input/output, display-memory, and filing-system tasks, leaving the second processor free to handle application programs, possibly running an entirely different operating system.

The second processor is a compact, four-layer printed-circuit board carrying an ARM processor in an 84-pin Jedec type-B package; it also contains 1 megabyte of dynamic random-access memory and a bootstrap ROM. Software furnished with the board includes a simple operating system, a multiple-window text editor, compilers for the BCPL and Modula 2 languages, and a Lisp interpreter. Compilers for C, Pascal, and Fortran, together with a version of Prolog, are expected to be completed later this year.

The ARM microprocessor



**IN SILICON.** The ARM chip, for the Acorn RISC machine, saw light in April as first-time-right silicon, thanks to computer-aided-design tools.